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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,061	08/17/2001	Jun Koyama	12732-070001	2600

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EXAMINER	
LIANG, REGINA	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/931,061	Applicant(s) KOYAMA ET AL.	
	Examiner Regina Liang	Art Unit 2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-61* is/are pending in the application.

4a) Of the above claim(s) *1-20,46-56 and 59-61* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-45,57 and 58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/2/05, 1/3/05, 12/10/04, 1/14/02, 8/17/01.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II, claims 21-45, 57, 58 in the reply filed on 12/17/04 is acknowledged.

2. This application contains claims 1-20, 46-56, 59-61 drawn to an invention nonelected without traverse in the reply filed on 12/17/04. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Drawings

3. Figures 13, 14, 19 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 21-45, 57, 58 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 21, "input electrodes of the n write-in transistors are each electrically connected to the source" (line 21) should be removed.

As to claim 33, line 6 from the bottom, "write-in" should be changed to –read-out--.

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 21-45, 57, 58 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 23-49 of copending Application No. 09/930,956. Although the conflicting claims are not identical, they are not patentably distinct from each other because both claims 21-45, 57 and 58 of this application and claims 23-49 of copending application are claiming a similar pixel memory structure and reading/writing control of the pixel memory in a display device.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

The following is an example for comparing claim 21 of this application and claim 23 of copending application.

Claim 21 of this application	Claim 23 of copending application 09/930,956
An electronic device comprising a plurality of pixels, each of the pixels having: a source signal line; n (where n is a natural number, n≥2) gate signal lines used for write-in; n gate signal lines used for read-out; n transistors used for write-in; n transistors used for read-out;	A light crystal display device having a plurality of pixels, each of the pixels having: a source signal line; n (n is a natural number, and satisfies 2≤n) writing gate signal lines; n reading gate signal lines; n writing transistors; n reading transistors;
n x m volatile memory circuits for storing m frame portions (where m is a natural number, m≥1) of an n-bit digital image signal; n x k non-volatile memory circuits for storing k frame portions (where k is a natural number, k≥1) of the n-bit digital image signal; 2n volatile memory circuit selection portions; 2n non-volatile memory circuit selection	n x m memory circuits for storing m (m is a natural number, and satisfies 1≤m) frames of n bit digital video signals; n x k non-volatile memory circuits for storing k (k is a natural number, and satisfies 1≤k) of the n bit digital video signal; 2n memory circuit selecting units; 2n non-volatile memory circuit selecting units;

portions;	
an electric current supply line; an EL driver transistor; and an EL element; wherein:	a liquid crystal element,
gate electrodes of the n write-in transistors are each electrically connected to any one of the n write-in gate signal lines, with each of said gate electrodes connected to a different write-in gate signal line;	wherein each gate electrode of the n writing transistors is electrically connected to one of the n writing gate signal lines, with no two gate electrodes sharing the same writing gate signal line,
input electrodes of the n write-in transistors are each electrically connected to the source signal line;	wherein each input electrode of the n writing transistors is electrically connected to the source signal line,
output electrodes of the n write-in transistors are each electrically connected to the volatile memory circuits through any one of the volatile memory circuit selection portions, with each of said output electrodes being connected through a different volatile memory circuit selection portion;	each output electrode of the n writing transistors is electrically connected to one of m circuits out of the n x m memory circuits through one of n units out of the 2n memory circuit selecting units, each memory circuit selecting unit making selection for no more than one output electrode,
the output electrodes of the n write-in transistors are each electrically connected to	wherein each output electrode of the n writing transistors is electrically connect to one of k

the non-volatile memory circuits through any one of the non-volatile memory circuit selection portions, with each of said output electrodes being connected through a different non-volatile memory circuit selection portion;	circuits out of the n x k non-volatile memory circuits through one of n units out of the 2n non-volatile memory circuit selecting units, each non-volatile memory circuit selecting unit making selection for no more than one output electrode,
gate electrodes of the n read-out transistors are each electrically connected to any one of the n read-out gate signal lines, with each of said gate electrodes connected to a different read-out gate signal line;	wherein each gate electrode of the n reading transistors is electrically connected to one of the n reading gate signal lines, with no two gate electrodes sharing the same reading gate signal line,
the input electrodes of the n read-out transistors are each electrically connected to the volatile memory circuits through any one of the volatile memory circuit selection portions, with each of said input electrodes being connected through a different volatile memory circuit selection portion;	wherein each input electrode of the n reading transistors is electrically connected to one of m circuits out of the n x m memory circuits through one of n units out of the 2n memory circuit selecting units, each memory circuit selecting unit making selection for no more than one input electrode,
the input electrodes of the n read-out transistors are each electrically connected to the non-volatile memory circuits through any one of the non-volatile memory circuit	Wherein each input electrode of the n reading transistors is electrically connected to one of k circuits out of the n x k non-volatile memory circuits though one of n units of the 2n non-

selection portions, with each of said input electrodes being connected though a different non-volatile memory circuit selection portion;	volatile memory circuit selecting units, each non-volatile memory circuit selecting unit making selection for no more than one input electrode, and
the output electrodes of the n read-out transistors are each electrically connected to a gate electrode of the EL driver transistor;	Wherein each output electrode of the n reading transistors is electrically connected to one of electrodes of the liquid crystal element.
an input electrode of the EL driver transistor is electrically connected to the electric current supply line; and	
an output electrode of the EL driver transistor is electrically connected to one electrode of the EL element.	

As can be seen above, claim 21 of this application is similar to claim 23 of copending application, the corresponding pixel memory structure and reading/writing method are the same. Claim 21 differs from claim 23 in that claim 21 recites the pixel element comprising EL element while claim 23 recites the pixel element is a liquid crystal element. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made that the pixel memory structure and functionality are factually independent from the display type.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Regina Liang whose telephone number is (571) 272-7693. The examiner can normally be reached on Monday-Friday from 8AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard, can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Regina Liang
Primary Examiner
Art Unit 2674

3/17/05